LH28F002SC-L/SCH-L

DESCRIPTION

The LH28F002SC-L/SCH-L flash memories with SmartVoltage technology are high-density, low-cost, nonvolatile, read/write storage solution for a wide range of applications. Their symmetrically-blocked architecture, flexible voltage and enhanced cycling capability provide for highly flexible component suitable for resident flash arrays, SIMMs and memory cards. Their enhanced capabilities provide for an ideal solution for code + data storage applications. For secure code storage applications, such as networking, where code is either directly executed out of flash or downloaded to DRAM, the LH28F002SC-L/SCH-L offer three levels of protection: absolute protection with VPP at GND, selective hardware block locking, or flexible software block locking. These alternatives give designers ultimate control of their code security needs.

FEATURES

- SmartVoltage technology
 - 2.7 V (Read-only), 3.3 V or 5 V Vcc
 - 3.3 V, 5 V or 12 V VPP
- High performance read access time LH28F002SC-L85/SCH-L85
 - 85 ns (5.0±0.25 V)/ 90 ns (5.0±0.5 V)/ 120 ns (3.3±0.3 V)/150 ns (2.7 to 3.6 V)
 LH28F002SC-L12/SCH-L12
 - 120 ns (5.0±0.5 V)/ 150 ns (3.3±0.3 V)/ 170 ns (2.7 to 3.6 V)

2 M-bit (256 kB x 8) SmartVoltage Flash Memories

- Enhanced automated suspend options
 - Byte write suspend to read
 - Block erase suspend to byte write
 - Block erase suspend to read
- · Enhanced data protection features
 - Absolute protection with VPP = GND
 - Flexible block locking
 - Block erase/byte write lockout during power transitions
- SRAM-compatible write interface
- · High-density symmetrically-blocked architecture
 - Four 64 k-byte erasable blocks
- Enhanced cycling capability
 - 100 000 block erase cycles
 - 0.4 million block erase cycles/chip
- Low power management
 - Deep power-down mode
 - Automatic power saving mode decreases Icc in static mode
- · Automated byte write and block erase
 - Command user interface
 - Status register
- ETOX^{TM*} V nonvolatile flash technology
- Packages
 - 40-pin TSOP Type I (TSOP040-P-1020)

Normal bend

44-pin SOP (SOP044-P-0600)

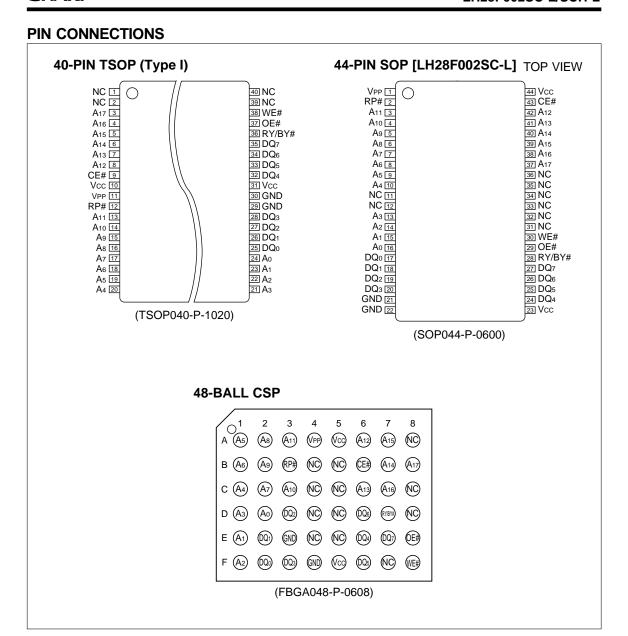
[LH28F002SC-L]

- 48-ball CSP (FBGA048-P-0608)

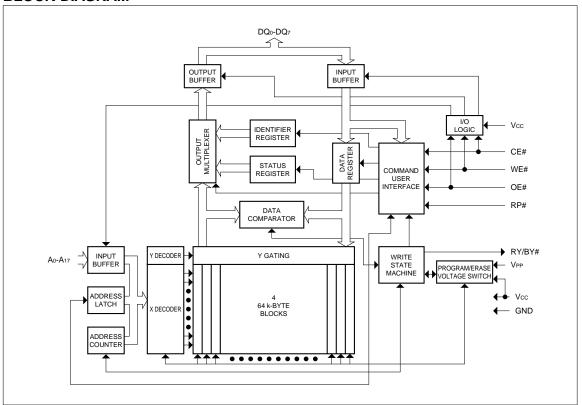
COMPARISON TABLE

VERSIONS	OPERATING TEMPERATURE	DC CHARACTERISTICS Vcc deep power-down current (MAX.)	PACKAGE
LH28F002SC-L	0 to +70°C	10 μA	40-pin TSOP (I), 44-pin SOP, 48-ball CSP
LH28F002SCH-L	-40 to +85°C	20 μΑ	40-pin TSOP (I), 48-ball CSP

^{*} ETOX is a trademark of Intel Corporation.



BLOCK DIAGRAM



SHARP

PIN DESCRIPTION

SYMBOL	TYPE	NAME AND FUNCTION
Λο Λ47	INPUT	ADDRESS INPUTS: Inputs for addresses during read and write operations. Addresses
A0-A17	INPUT	are internally latched during a write cycle.
		DATA INPUT/OUTPUTS: Inputs data and commands during CUI write cycles; outputs
DO: DO-	INPUT/	data during memory array, status register, and identifier code read cycles. Data pins
DQ0-DQ7	DQ ₀ -DQ ₇ OUTPUT	float to high-impedance when the chip is deselected or outputs are disabled. Data is
		internally latched during a write cycle.
		CHIP ENABLE: Activates the device's control logic, input buffers, decoders, and sense
CE#	INPUT	amplifiers. CE#-high deselects the device and reduces power consumption to standby
		levels.
		RESET/DEEP POWER-DOWN: Puts the device in deep power-down mode and resets
		internal automation. RP#-high enables normal operation. When driven low, RP# inhibits
		write operations which provide data protection during power transitions. Exit from deep
	IN IDI IT	power-down sets the device to read array mode. RP# at VHH enables setting of the
RP#	INPUT	master lock-bit and enables configuration of block lock-bits when the master lock-bit is
		set. RP# = Vhh overrides block lock-bits thereby enabling block erase and byte write
		operations to locked memory blocks. Block erase, byte write, or lock-bit configuration
		with VIH ≤ RP# ≤ VHH produce spurious results and should not be attempted.
OE#	INPUT	OUTPUT ENABLE: Gates the device's outputs during a read cycle.
\A/E-#	INDLIT	WRITE ENABLE: Controls writes to the CUI and array blocks. Addresses and data are
WE#	INPUT	latched on the rising edge of the WE# pulse.
		READY/BUSY: Indicates the status of the internal WSM. When low, the WSM is
		performing an internal operation (block erase, byte write, or lock-bit configuration).
53.453.44		RY/BY#-high indicates that the WSM is ready for new commands, block erase is
RY/BY#	OUTPUT	suspended, and byte write is inactive, byte write is suspended, or the device is in deep
		power-down mode. RY/BY# is always active and does not float when the chip is
		deselected or data outputs are disabled.
		BLOCK ERASE, BYTE WRITE, LOCK-BIT CONFIGURATION POWER SUPPLY : For
		erasing array blocks, writing bytes, or configuring lock-bits. With VPP ≤ VPPLK, memory
VPP	SUPPLY	contents cannot be altered. Block erase, byte write, and lock-bit configuration with an
		invalid VPP (see Section 6.2.3 "DC CHARACTERISTICS") produce spurious results
		and should not be attempted.
		DEVICE POWER SUPPLY: Internal detection configures the device for 2.7 V, 3.3 V or
		5 V operation. To switch from one voltage to another, ramp Vcc down to GND and then
	Vcc SUPPLY	ramp Vcc to the new voltage. Do not float any power pins. With Vcc ≤ VLKo, all write
Vcc		attempts to the flash memory are inhibited. Device operations at invalid Vcc voltage
		(see Section 6.2.3 "DC CHARACTERISTICS") produce spurious results and should
		not be attempted. Block erase, byte write and lock-bit configuration operations with Vcc
		< 3.0 V are not supported.
GND	SUPPLY	GROUND: Do not float any ground pins.
NC		NO CONNECT: Lead is not internal connected; recommend to be floated.

1 INTRODUCTION

This datasheet contains LH28F002SC-L/SCH-L specifications. Section 1 provides a flash memory overview. Sections 2, 3, 4, and 5 describe the memory organization and functionality. Section 6 covers electrical specifications. LH28F002SC-L/SCH-L flash memories documentation also includes ordering information which is referenced in Section 7.

1.1 New Features

The LH28F002SC-L/SCH-L SmartVoltage flash memories maintain backwards-compatibility with the LH28F008SA. Key enhancements over the LH28F008SA include:

- SmartVoltage Technology
- Enhanced Suspend Capabilities
- In-System Block Locking

Both devices share a compatible pinout, status register, and software command set. These similarities enable a clean upgrade from the LH28F008SA to LH28F002SC-L/SCH-L. When upgrading, it is important to note the following differences:

- Because of new feature support, the two devices have different device codes. This allows for software optimization.
- VPPLK has been lowered from 6.5 V to 1.5 V to support 3.3 V and 5 V block erase, byte write, and lock-bit configuration operations. Designs that switch VPP off during read operations should make sure that the VPP voltage transitions to GND.
- To take advantage of SmartVoltage technology, allow VPP connection to 3.3 V or 5 V.

1.2 Product Overview

The LH28F002SC-L/SCH-L are high-performance 2 M-bit SmartVoltage flash memories organized as 256 k-byte of 8 bits. The 256 k-byte of data is arranged in four 64 k-byte blocks which are

individually erasable, lockable, and unlockable insystem. The memory map is shown in **Fig. 1**.

SmartVoltage technology provides a choice of Vcc and VPP combinations, as shown in **Table 1**, to meet system performance and power expectations. 2.7 V Vcc consumes approximately one-fifth the power of 5 V Vcc and 3.3 V Vcc consumes approximately one-fourth the power of 5 V Vcc. But, 5 V Vcc provides the highest read performance. VPP at 3.3 V and 5 V eliminates the need for a separate 12 V converter, while VPP = 12 V maximizes block erase and byte write performance. In addition to flexible erase and program voltages, the dedicated VPP pin gives complete data protection when VPP ≤ VPPLK.

Table 1 Vcc and VPP Voltage Combinations
Offered by SmartVoltage Technology

Vcc VOLTAGE	VPP VOLTAGE
2.7 V (NOTE 1)	_
3.3 V	3.3 V, 5 V, 12 V
5 V	5 V, 12 V

NOTE:

 Block erase, byte write and lock-bit configuration operations with Vcc < 3.0 V are not supported.

Internal Vcc and VPP detection circuitry automatically configures the device for optimized read and write operations.

A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase, byte write, and lock-bit configuration operations.

A block erase operation erases one of the device's 64 k-byte blocks typically within 1 second (5 V VCC,

12 V VPP) independent of other blocks. Each block can be independently erased 100 000 times (0.4 million block erases per device). Block erase suspend mode allows system software to suspend block erase to read data from, or write data to any other block.

Writing memory data is performed in byte increments typically within 6 μ s (5 V Vcc, 12 V VPP). Byte write suspend mode enables the system to read data from, or write data to any other flash memory array location.

Individual block locking uses a combination of bits, four block lock-bits and a master lock-bit, to lock and unlock blocks. Block lock-bits gate block erase and byte write operations, while the master lock-bit gates block lock-bit modification. Lock-bit configuration operations (Set Block Lock-Bit, Set Master Lock-Bit, and Clear Block Lock-Bits commands) set and cleared lock-bits.

The status register indicates when the WSM's block erase, byte write, or lock-bit configuration operation is finished.

The RY/BY# output gives an additional indicator of WSM activity by providing both a hardware signal of status (versus software polling) and status masking (interrupt masking for background block erase, for example). Status polling using RY/BY# minimizes both CPU overhead and system power consumption. When low, RY/BY# indicates that the WSM is performing a block erase, byte write, or lock-bit configuration. RY/BY#-high indicates that the WSM is ready for a new command, block erase is suspended (and byte write is inactive), byte write is suspended, or the device is in deep power-down mode.

The access time is 85 ns (tavqv) at the Vcc supply voltage range of 4.75 to 5.25 V over the temperature range, 0 to $+70^{\circ}$ C (LH28F002SC-L)/-40 to $+85^{\circ}$ C (LH28F002SCH-L). At 4.5 to 5.5 V Vcc, the access time is 90 ns or 120 ns. At lower Vcc voltage, the access time is 120 ns or 150 ns (3.0 to 3.6 V) and 150 ns or 170 ns (2.7 to 3.6 V).

The Automatic Power Saving (APS) feature substantially reduces active current when the device is in static mode (addresses not switching). In APS mode, the typical ICCR current is 1 mA at 5 V Vcc and 3 mA at 2.7 V and 3.3 V Vcc.

When CE# and RP# pins are at Vcc, the Icc CMOS standby mode is enabled. When the RP# pin is at GND, deep power-down mode is enabled which minimizes power consumption and provides write protection during reset. A reset time (tPHQV) is required from RP# switching high until outputs are valid. Likewise, the device has a wake time (tPHEL) from RP#-high until writes to the CUI are recognized. With RP# at GND, the WSM is reset and the status register is cleared.

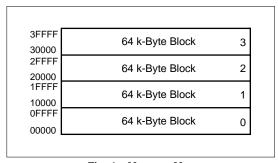


Fig. 1 Memory Map

2 PRINCIPLES OF OPERATION

The LH28F002SC-L/SCH-L SmartVoltage flash memories include an on-chip WSM to manage block erase, byte write, and lock-bit configuration functions. It allows for : 100% TTL-level control inputs, fixed power supplies during block erasure, byte write, and lock-bit configuration, and minimal processor overhead with RAM-like interface timings.

After initial device power-up or return from deep power-down mode (see **Table 2 "Bus Operations"**), the device defaults to read array mode. Manipulation of external memory control pins allow array read, standby, and output disable operations.

Status register and identifier codes can be accessed through the CUI independent of the VPP voltage. High voltage on VPP enables successful block erasure, byte writing, and lock-bit configuration. All functions associated with altering memory contents—block erase, byte write, lock-bit configuration, status, and identifier codes—are accessed via the CUI and verified through the status register.

Commands are written using standard microprocessor write timings. The CUI contents serve as input to the WSM, which controls the block erase, byte write, and lock-bit configuration. The internal algorithms are regulated by the WSM, including pulse repetition, internal verification, and margining of data. Addresses and data are internally latched during write cycles. Writing the appropriate command outputs array data, accesses the identifier codes, or outputs status register data.

Interface software that initiates and polls progress of block erase, byte write, and lock-bit configuration can be stored in any block. This code is copied to and executed from system RAM during flash memory updates. After successful completion, reads are again possible via the Read Array command. Block erase suspend allows system

software to suspend a block erase to read/write data from/to blocks other than that which is suspended. Byte write suspend allows system software to suspend a byte write to read data from any other flash memory array location.

2.1 Data Protection

Depending on the application, the system designer may choose to make the VPP power supply switchable (available only when memory block erases, byte writes, or lock-bit configurations are required) or hardwired to VPPH1/2/3. The device accommodates either design practice and encourages optimization of the processor-memory interface.

When VPP ≤ VPPLK, memory contents cannot be altered. The CUI, with two-step block erase, byte write, or lock-bit configuration command sequences, provides protection from unwanted operations even when high voltage is applied to VPP. All write functions are disabled when Vcc is below the write lockout voltage VLKO or when RP# is at VIL. The device's block locking capability provides additional protection from inadvertent code or data alteration by gating erase and byte write operations.

3 BUS OPERATION

The local CPU reads and writes flash memory insystem. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

3.1 Read

Information can be read from any block, identifier codes, or status register independent of the VPP voltage. RP# can be at either VIH or VHH.

The first task is to write the appropriate read mode command (Read Array, Read Identifier Codes, or Read Status Register) to the CUI. Upon initial device power-up or after exit from deep power-down mode, the device automatically resets to read

array mode. Four control pins dictate the data flow in and out of the component: CE#, OE#, WE#, and RP#. CE# and OE# must be driven active to obtain data at the outputs. CE# is the device selection control, and when active enables the selected memory device. OE# is the data output (DQ0-DQ7) control and when active drives the selected memory data onto the I/O bus. WE# must be at VIH and RP# must be at VIH or VHH. Fig. 13 illustrates a read cycle.

3.2 Output Disable

With OE# at a logic-high level (VIH), the device outputs are disabled. Output pins DQ0-DQ7 are placed in a high-impedance state.

3.3 Standby

CE# at a logic-high level (VIH) places the device in standby mode which substantially reduces device power consumption. DQo-DQ7 outputs are placed in a high-impedance state independent of OE#. If deselected during block erase, byte write, or lock-bit configuration, the device continues functioning, and consuming active power until the operation completes.

3.4 Deep Power-Down

RP# at VIL initiates the deep power-down mode.

In read modes, RP#-low deselects the memory, places output drivers in a high-impedance state and turns off all internal circuits. RP# must be held low for a minimum of 100 ns. Time tphqv is required after return from power-down until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI is reset to read array mode and status register is set to 80H.

During block erase, byte write, or lock-bit configuration modes, RP#-low will abort the operation. RY/BY# remains low until the reset operation is complete. Memory contents being altered are no longer valid; the data may be partially erased or written. Time tPHWL is required after RP# goes to logic-high (VIH) before another command can be written.

As with any automated device, it is important to assert RP# during system reset. When the system comes out of reset, it expects to read from the flash memory. Automated flash memories provide status information when accessed during block erase, byte write, or lock-bit configuration modes. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. SHARP's flash memories allow proper CPU initialization following a system reset through the use of the RP# input. In this application, RP# is controlled by the same RESET# signal that resets the system CPU.

3.5 Read Identifier Codes Operation

The read identifier codes operation outputs the manufacture code, device code, block lock configuration codes for each block, and the master lock configuration code (see **Fig. 2**). Using the manufacture and device codes, the system CPU can automatically match the device with its proper algorithms. The block lock and master lock configuration codes identify locked and unlocked blocks and master lock-bit setting.

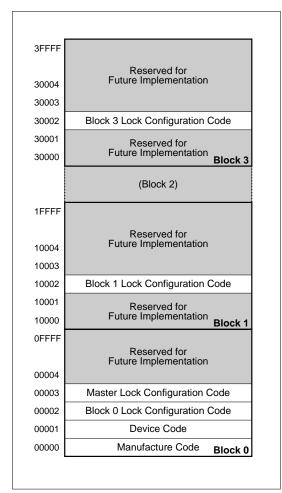


Fig. 2 Device Identifier Code Memory Map

3.6 Write

Writing commands to the CUI enable reading of device data and identifier codes. They also control inspection and clearing of the status register. When VPP = VPPH1/2/3, the CUI additionally controls block erasure, byte write, and lock-bit configuration.

The Block Erase command requires appropriate command data and an address within the block to be erased. The Byte Write command requires the command and address of the location to be written. Set Master and Block Lock-Bit commands require the command and address within the device (Master Lock) or block within the device (Block Lock) to be locked. The Clear Block Lock-Bits command requires the command and address within the device.

The CUI does not occupy an addressable memory location. It is written when WE# and CE# are active. The address and data needed to execute a command are latched on the rising edge of WE# or CE# (whichever goes high first). Standard microprocessor write timings are used. Fig. 14 and Fig. 15 illustrate WE# and CE#-controlled write operations.

4 COMMAND DEFINITIONS

When the VPP voltage \leq VPPLK, read operations from the status register, identifier codes, or blocks are enabled. Placing VPPH1/2/3 on VPP enables successful block erase, byte write and lock-bit configuration operations.

Device operations are selected by writing specific commands into the CUI. **Table 3** defines these commands.

				•					
MODE	NOTE	RP#	CE#	OE#	WE#	ADDRESS	VPP	DQ ₀₋₇	RY/BY#
Read	1, 2, 3, 8	VIH or VHH	VIL	VIL	ViH	Х	Х	Dout	Х
Output Disable	3	VIH or VHH	VIL	ViH	ViH	Х	Х	High Z	Х
Standby	3	VIH or VHH	ViH	Х	Х	Х	Х	High Z	Х
Deep Power-Down	4	VIL	Х	Х	X	Х	Χ	High Z	Vон
Read Identifier Codes	8	VIH or VHH	VIL	VIL	ViH	See Fig. 2	Х	(NOTE 5)	Voн
Write	3, 6, 7, 8	VIH or VHH	VIL	ViH	VIL	Х	Х	DIN	Х

Table 2 Bus Operations

- Refer to Section 6.2.3 "DC CHARACTERISTICS".
 When VPP ≤ VPPLK, memory contents can be read, but not altered.
- X can be VIL or VIH for control pins and addresses, and VPPLK or VPPH1/2/3 for VPP. See Section 6.2.3 "DC CHARACTERISTICS" for VPPLK and VPPH1/2/3 voltages.
- RY/BY# is VoL when the WSM is executing internal block erase, byte write, or lock-bit configuration algorithms. It is VoH during when the WSM is not busy, in block erase suspend mode (with byte write inactive), byte write suspend mode, or deep power-down mode.
- RP# at GND±0.2 V ensures the lowest deep powerdown current.
- 5. See Section 4.2 for read identifier code data.
- Command writes involving block erase, byte write, or lock-bit configuration are reliably executed when VPP = VPPH1/2/3 and VCC = VCC2/3/4. Block erase, byte write, or lock-bit configuration with VCC < 3.0 V or VIH < RP# < VHH produce spurious results and should not be attempted.
- 7. Refer to **Table 3** for valid DIN during a write operation.
- 8. Don't use the timing both OE# and WE# are VIL.

COMMAND	BUS CYCLES	ES FIRST BUS CYCLE			/CLE	SECOND BUS CYCLE		
COMMAND	REQ'D.	NOTE	Oper (NOTE 1)	Addr (NOTE 2)	Data (NOTE 3)	Oper (NOTE 1)	Addr (NOTE 2)	Data (NOTE 3)
Read Array/Reset	1		Write	Х	FFH			
Read Identifier Codes	≥ 2	4	Write	Х	90H	Read	IA	ID
Read Status Register	2		Write	Х	70H	Read	Х	SRD
Clear Status Register	1		Write	Х	50H			
Block Erase	2	5	Write	BA	20H	Write	BA	D0H
Byte Write	2	5, 6	Write	WA	40H or 10H	Write	WA	WD
Block Erase and	4	5	Write	Х	B0H			
Byte Write Suspend	') 5	vvrite	^	ВОП			
Block Erase and	4	5	Write	Х	DOLL			
Byte Write Resume	') 5	vvrite	^	D0H			
Set Block Lock-Bit	2	7	Write	BA	60H	Write	BA	01H
Set Master Lock-Bit	2	7	Write	Х	60H	Write	Х	F1H
Clear Block Lock-Bits	2	8	Write	Х	60H	Write	Х	D0H

Table 3 Command Definitions (NOTE 9)

- 1. Bus operations are defined in Table 2.
- 2. $X = Any \ valid \ address \ within the device.$
 - IA = Identifier code address : see Fig. 2.
 - BA = Address within the block being erased or locked.
 - WA = Address of memory location to be written.
- SRD = Data read from status register. See Table 6 for a description of the status register bits.
 - WD = Data to be written at location WA. Data is latched on the rising edge of WE# or CE# (whichever goes high first).
 - ID = Data read from identifier codes.
- Following the Read Identifier Codes command, read operations access manufacture, device, block lock, and master lock codes. See Section 4.2 for read identifier code data.
- If the block is locked, RP# must be at VHH to enable block erase or byte write operations. Attempts to issue a block erase or byte write to a locked block while RP# is VIH.

- Either 40H or 10H is recognized by the WSM as the byte write setup.
- If the master lock-bit is set, RP# must be at VHH to set a block lock-bit. RP# must be at VHH to set the master lock-bit. If the master lock-bit is not set, a block lock-bit can be set while RP# is VIH.
- If the master lock-bit is set, RP# must be at VHH to clear block lock-bits. The clear block lock-bits operation simultaneously clears all block lock-bits. If the master lock-bit is not set, the Clear Block Lock-Bits command can be done while RP# is VIH.
- Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

SHARP LH28F002SC-L/SCH-L

4.1 Read Array Command

Upon initial device power-up and after exit from deep power-down mode, the device defaults to read array mode. This operation is also initiated by writing the Read Array command. The device remains enabled for reads until another command is written. Once the internal WSM has started a block erase, byte write or lock-bit configuration, the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via an Erase Suspend or Byte Write Suspend command. The Read Array command functions independently of the VPP voltage and RP# can be VIH or VHH.

4.2 Read Identifier Codes Command

The identifier code operation is initiated by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in **Fig. 2** retrieve the manufacture, device, block lock configuration and master lock configuration codes (see **Table 4** for identifier code values). To terminate the operation, write another valid command. Like the Read Array command, the Read Identifier Codes command functions independently of the VPP voltage and RP# can be VIH or VHH. Following the Read Identifier Codes command, the following information can be read:

CODE	ADDRESS	DATA
Manufacture Code	00000H	B0
Device Code	00001H	34
Block Lock Configuration	X0002H (NOTE 1)	
Block is Unlocked		$DQ_0 = 0$
Block is Locked		DQ0 = 1
Reserved for Future Use		DQ1-7
Master Lock Configuration	00003H	
Device is Unlocked		$DQ_0 = 0$
Device is Locked		DQ0 = 1
Reserved for Future Use		DQ1-7

Table 4 Identifier Codes

NOTE:

 X selects the specific block lock configuration code to be read. See Fig. 2 for the device identifier code memory map.

4.3 Read Status Register Command

The status register may be read to determine when a block erase, byte write, or lock-bit configuration is complete and whether the operation completed successfully. It may be read at any time by writing the Read Status Register command. After writing this command, all subsequent read operations output data from the status register until another valid command is written. The status register contents are latched on the falling edge of OE# or CE#, whichever occurs. OE# or CE# must toggle to VIH before further reads to update the status register latch. The Read Status Register command functions independently of the VPP voltage. RP# can be VIH or VHH.

4.4 Clear Status Register Command

Status register bits SR.5, SR.4, SR.3, and SR.1 are set to "1"s by the WSM and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see **Table 6**). By allowing system software to reset these bits, several operations (such as cumulatively erasing or locking multiple blocks or writing several bytes in sequence) may be performed. The status register may be polled to determine if an error occurred during the sequence.

To clear the status register, the Clear Status Register command (50H) is written. It functions independently of the applied VPP voltage. RP# can be VIH or VHH. This command is not functional during block erase or byte write suspend modes.

4.5 Block Erase Command

Erase is executed one block at a time and initiated by a two-cycle command. A block erase setup is first written, followed by a block erase confirm. This command sequence requires appropriate sequencing and an address within the block to be erased (erase changes all block data to FFH). Block preconditioning, erase, and verify are handled internally by the WSM (invisible to the system). After the two-cycle block erase sequence is written,

the device automatically outputs status register data when read (see **Fig. 3**). The CPU can detect block erase completion by analyzing the output data of the RY/BY# pin or status register bit SR.7.

When the block erase is complete, status register bit SR.5 should be checked. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1". Also, reliable block erasure can only occur when Vcc = VCC2/3/4 and VPP = VPPH1/2/3. In the absence of this high voltage, block contents are protected against erasure. If block erase is attempted while VPP ≤ VPPLK, SR.3 and SR.5 will be set to "1". Successful block erase requires that the corresponding block lock-bit be cleared or, if set, that RP# = VHH. If block erase is attempted when the corresponding block lock-bit is set and RP# = VIH, SR.1 and SR.5 will be set to "1". Block erase operations with VIH < RP# < VHH produce spurious results and should not be attempted.

4.6 Byte Write Command

Byte write is executed by a two-cycle command sequence. Byte write setup (standard 40H or alternate 10H) is written, followed by a second write that specifies the address and data (latched on the rising edge of WE#). The WSM then takes over, controlling the byte write and write verify algorithms internally. After the byte write sequence is written, the device automatically outputs status register data when read (see **Fig. 4**). The CPU can detect the completion of the byte write event by analyzing the RY/BY# pin or status register bit SR.7.

When byte write is complete, status register bit SR.4 should be checked. If byte write error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully write to "0"s. The CUI remains in read status register mode until it receives another command.

Reliable byte writes can only occur when VCC = VCC2/3/4 and VPP = VPPH1/2/3. In the absence of this high voltage, memory contents are protected against byte writes. If byte write is attempted while VPP \leq VPPLK, status register bits SR.3 and SR.4 will be set to "1". Successful byte write requires that the corresponding block lock-bit be cleared or, if set, that RP# = VHH. If byte write is attempted when the corresponding block lock-bit is set and RP# = VIH, SR.1 and SR.4 will be set to "1". Byte write operations with VIH < RP# < VHH produce spurious results and should not be attempted.

4.7 Block Erase Suspend Command

The Block Erase Suspend command allows block erase interruption to read or byte write data in another block of memory. Once the block erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. The device outputs status register data when read after the Block Erase Suspend command is written. Polling status register bits SR.7 and SR.6 can determine when the block erase operation has been suspended (both will be set to "1"). RY/BY# will also transition to VOH. Specification twhRH2 defines the block erase suspend latency.

At this point, a Read Array command can be written to read data from blocks other than that which is suspended. A Byte Write command sequence can also be issued during erase suspend to program data in other blocks. Using the Byte

SHARP LH28F002SC-L/SCH-L

Write Suspend command (see **Section 4.8**), a byte write operation can also be suspended. During a byte write operation with block erase suspended, status register bit SR.7 will return to "0" and the RY/BY# output will transition to Vol. However, SR.6 will remain "1" to indicate block erase suspend status.

The only other valid commands while block erase is suspended are Read Status Register and Block Erase Resume. After a Block Erase Resume command is written to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and RY/BY# will return to Vol. After the Erase Resume command is written, the device automatically outputs status register data when read (see Fig. 5). VPP must remain at VPPH1/2/3 (the same VPP level used for block erase) while block erase is suspended. RP# must also remain at VIH or VHH (the same RP# level used for block erase). Block erase cannot resume until byte write operations initiated during block erase suspend have completed.

4.8 Byte Write Suspend Command

The Byte Write Suspend command allows byte write interruption to read data in other flash memory locations. Once the byte write process starts, writing the Byte Write Suspend command requests that the WSM suspend the byte write sequence at a predetermined point in the algorithm. The device continues to output status register data when read after the Byte Write Suspend command is written. Polling status register bits SR.7 and SR.2 can determine when the byte write operation has been suspended (both will be set to "1"). RY/BY# will also transition to Voh. Specification twhrhat defines the byte write suspend latency.

At this point, a Read Array command can be written to read data from locations other than that which is suspended. The only other valid

commands while byte write is suspended are Read Status Register and Byte Write Resume. After Byte Write Resume command is written to the flash memory, the WSM will continue the byte write process. Status register bits SR.2 and SR.7 will automatically clear and RY/BY# will return to Vol. After the Byte Write Resume command is written, the device automatically outputs status register data when read (see **Fig. 6**). VPP must remain at VPPH1/2/3 (the same VPP level used for byte write) while in byte write suspend mode. RP# must also remain at VIH or VHH (the same RP# level used for byte write).

4.9 Set Block and Master Lock-Bit Commands

A flexible block locking and unlocking scheme is enabled via a combination of block lock-bits and a master lock-bit. The block lock-bits gate program and erase operations while the master lock-bit gates block-lock bit modification. With the master lock-bit not set, individual block lock-bits can be set using the Set Block Lock-Bit command. The Set Master Lock-Bit command, in conjunction with RP# = VHH, sets the master lock-bit. After the master lock-bit is set, subsequent setting of block lock-bits requires both the Set Block Lock-Bit command and VHH on the RP# pin. See **Table 5** for a summary of hardware and software write protection options.

Set block lock-bit and master lock-bit are executed by a two-cycle command sequence. The set block or master lock-bit setup along with appropriate block or device address is written followed by either the set block lock-bit confirm (and an address within the block to be locked) or the set master lock-bit confirm (and any device address). The WSM then controls the set lock-bit algorithm. After the sequence is written, the device automatically outputs status register data when read (see Fig. 7). The CPU can detect the completion of the set lock-bit event by analyzing the RY/BY# pin output or status register bit SR.7.

When the set lock-bit operation is complete, status register bit SR.4 should be checked. If an error is detected, the status register should be cleared. The CUI will remain in read status register mode until a new command is issued.

This two-step sequence of set-up followed by execution ensures that lock-bits are not accidentally set. An invalid Set Block or Master Lock-Bit command will result in status register bits SR.4 and SR.5 being set to "1". Also, reliable operations occur only when Vcc = Vcc2/3/4 and VPP = VPPH1/2/3. In the absence of this high voltage, lock-bit contents are protected against alteration.

A successful set block lock-bit operation requires that the master lock-bit be cleared or, if the master lock-bit is set, that RP# = Vhh. If it is attempted with the master lock-bit set and RP# = Vih, SR.1 and SR.4 will be set to "1" and the operation will fail. Set block lock-bit operations while Vih < RP# < Vhh produce spurious results and should not be attempted. A successful set master lock-bit operation requires that RP# = Vhh. If it is attempted with RP# = Vih, SR.1 and SR.4 will be set to "1" and the operation will fail. Set master lock-bit operations with Vih < RP# < Vhh produce spurious results and should not be attempted.

4.10 Clear Block Lock-Bits Command

All set block lock-bits are cleared in parallel via the Clear Block Lock-Bits command. With the master lock-bit not set, block lock-bits can be cleared using only the Clear Block Lock-Bits command. If the master lock-bit is set, clearing block lock-bits requires both the Clear Block Lock-Bits command and VHH on the RP# pin. See **Table 5** for a summary of hardware and software write protection options.

Clear block lock-bits operation is executed by a two-cycle command sequence. A clear block lockbits setup is first written. After the command is written, the device automatically outputs status register data when read (see **Fig. 8**). The CPU can detect completion of the clear block lock-bits event by analyzing the RY/BY# pin output or status register bit SR.7.

When the operation is complete, status register bit SR.5 should be checked. If a clear block lock-bits error is detected, the status register should be cleared. The CUI will remain in read status register mode until another command is issued.

This two-step sequence of set-up followed by execution ensures that block lock-bits are not accidentally cleared. An invalid Clear Block Lock-Bits command sequence will result in status register bits SR.4 and SR.5 being set to "1". Also, a reliable clear block lock-bits operation can only occur when VCC = VCC2/3/4 and VPP = VPPH1/2/3. If a clear block lock-bits operation is attempted while VPP ≤ VPPLK, SR.3 and SR.5 will be set to "1". In the absence of this high voltage, the block lock-bit contents are protected against alteration. A successful clear block lock-bits operation requires that the master lock-bit is not set or, if the master lock-bit is set, that RP# = VHH. If it is attempted with the master lock-bit set and RP# = VIH, SR.1 and SR.5 will be set to "1" and the operation will fail. A clear block lock-bits operation with VIH < RP# < VHH produce spurious results and should not be attempted.

If a clear block lock-bits operation is aborted due to VPP or Vcc transition out of valid range or RP# active transition, block lock-bit values are left in an undetermined state. A repeat of clear block lock-bits is required to initialize block lock-bit contents to known values. Once the master lock-bit is set, it cannot be cleared.

Table 5	Write	Drotoction	Alternatives
l able 5	vvrite	Protection	Alternatives

OPERATION	MASTER LOCK-BIT	BLOCK LOCK-BIT	RP#	EFFECT
Block Erase		0	VIH or VHH	Block Erase and Byte Write Enabled
or Byte Write	X	1	Vih	Block is Locked. Block Erase and Byte Write Disabled
or byte write	3 1	VHH	Block Lock-Bit Override. Block Erase and Byte Write Enabled	
Set Block	0	Х	VIH or VHH	Set Block Lock-Bit Enabled
Lock-Bit	4	X	ViH	Master Lock-Bit is Set. Set Block Lock-Bit Disabled
LOCK-DIL		^	VHH	Master Lock-Bit Override. Set Block Lock-Bit Enabled
Set Master	Х	Х	VIH	Set Master Lock-Bit Disabled
Lock-Bit	^	^	VHH	Set Master Lock-Bit Enabled
Class Black	0	Х	VIH or VHH	Clear Block Lock-Bits Enabled
Clear Block	4	Х	ViH	Master Lock-Bit is Set. Clear Block Lock-Bits Disabled
Lock-Bits	l	, X	VHH	Master Lock-Bit Override. Clear Block Lock-Bits Enabled

Table 6 Status Register Definition

WSMS	ESS	ECLBS	BWSLBS	VPPS	BWSS	DPS	R
7	6	5	4	3	2	1	0

SR.7 = WRITE STATE MACHINE STATUS (WSMS)

1 = Ready

0 = Busy

SR.6 = ERASE SUSPEND STATUS (ESS)

1 = Block Erase Suspended

0 = Block Erase in Progress/Completed

SR.5 = ERASE AND CLEAR LOCK-BITS STATUS (ECLBS)

1 = Error in Block Erase or Clear Lock-Bits

0 = Successful Block Erase or Clear Lock-Bits

SR.4 = BYTE WRITE AND SET LOCK-BIT STATUS (BWSLBS)

1 = Error in Byte Write or Set Master/Block Lock-Bit

0 = Successful Byte Write or Set Master/Block Lock-Bit

SR.3 = VPP STATUS (VPPS)

1 = VPP Low Detect, Operation Abort

0 = VPP OK

SR.2 = BYTE WRITE SUSPEND STATUS (BWSS)

1 = Byte Write Suspended

0 = Byte Write in Progress/Completed

SR.1 = DEVICE PROTECT STATUS (DPS)

1 = Master Lock-Bit, Block Lock-Bit and/or RP# Lock Detected, Operation Abort

0 = Unlock

SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

NOTES:

Check RY/BY# or SR.7 to determine block erase, byte write, or lock-bit configuration completion.

SR.6-0 are invalid while SR.7 = "0".

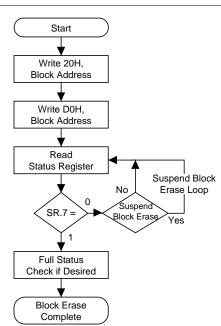
If both SR.5 and SR.4 are "1"s after a block erase or lock-bit configuration attempt, an improper command sequence was entered.

SR.3 does not provide a continuous indication of VPP level. The WSM interrogates and indicates the VPP level only after Block Erase, Byte Write, Set Block/Master Lock-Bit, or Clear Block Lock-Bits command sequences.

SR.3 is not guaranteed to reports accurate feedback only when $VPP \neq VPPH1/2/3$.

SR.1 does not provide a continuous indication of master and block lock-bit values. The WSM interrogates the master lock-bit, block lock-bit, and RP# only after Block Erase, Byte Write, or Lock-Bit configuration command sequences. It informs the system, depending on the attempted operation, if the block lock-bit is set, master lock-bit is set, and/or RP# is not Vhh. Reading the block lock and master lock configuration codes after writing the Read Identifier Codes command indicates master and block lock-bit status.

SR.0 is reserved for future use and should be masked out when polling the status register.



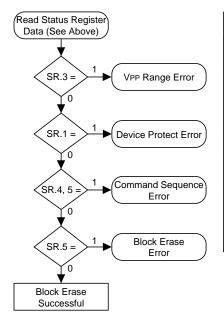
BUS OPERATION	COMMAND	COMMENTS
Write	Erase Setup	Data = 20H Addr = Within Block to be Erased
Write	Erase Confirm	Data = D0H Addr = Within Block to be Erased
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent block erasures.

Full status check can be done after each block erase or after a sequence of block erasures.

Write FFH after the last block erase operation to place device in read array mode.

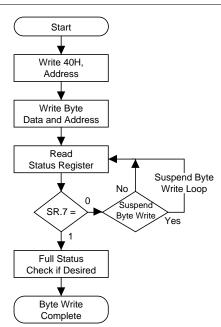
FULL STATUS CHECK PROCEDURE



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR.3 1 = VPP Error Detect
Standby		Check SR.1 1 = Device Protect Detect RP# = VIH, Block Lock-Bit is Set Only required for systems implementing lock-bit configuration
Standby		Check SR.4, 5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Block Erase Error

SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple blocks are erased before full status is checked.

Fig. 3 Automated Block Erase Flowchart



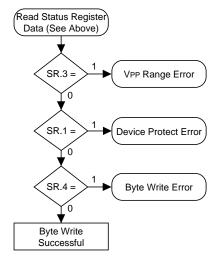
BUS OPERATION	COMMAND	COMMENTS
Write	Setup Byte Write	Data = 40H Addr = Location to be Written
Write	Byte Write	Data = Data to be Written Addr = Location to be Written
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent byte writes.

SR full status check can be done after each byte write or after a sequence of byte writes.

Write FFH after the last byte write operation to place device in read array mode.

FULL STATUS CHECK PROCEDURE



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR.3 1 = VPP Error Detect
Standby		Check SR.1 1 = Device Protect Detect RP# = VIH, Block Lock-Bit is Set Only required for systems implementing lock-bit configuration
Standby		Check SR.4 1 = Data Write Error

SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are written before full status is checked.

Fig. 4 Automated Byte Write Flowchart

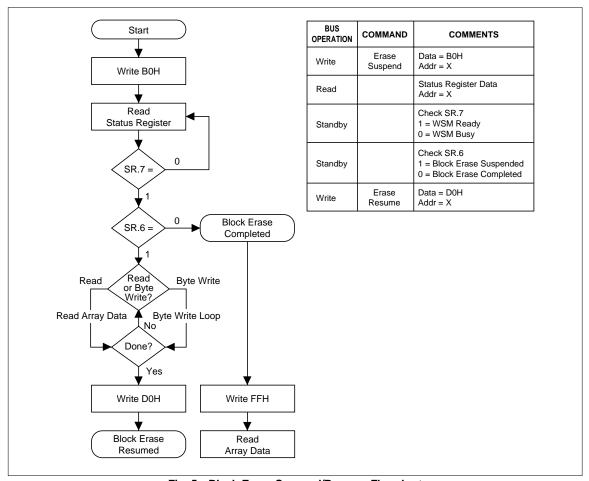


Fig. 5 Block Erase Suspend/Resume Flowchart

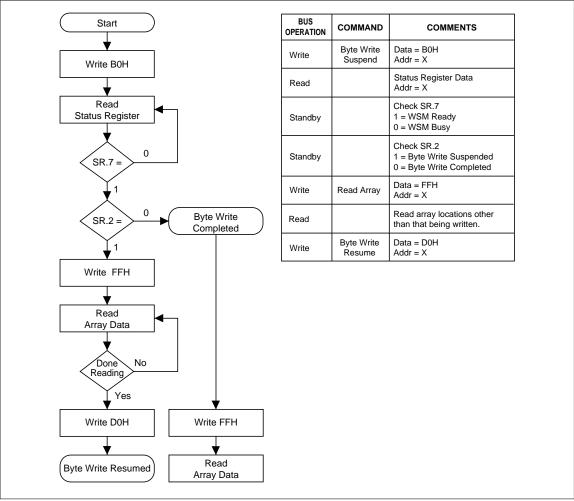
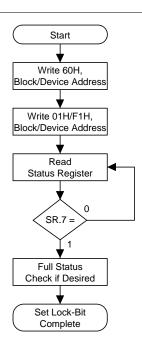


Fig. 6 Byte Write Suspend/Resume Flowchart



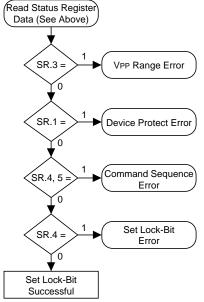
BUS OPERATION	COMMAND	COMMENTS
Write	Set Block/Master Lock-Bit Setup	Data = 60H Addr = Block Address (Block), Device Address (Master)
Write	Set Block or Master Lock-Bit Confirm	Data = 01H (Block), F1H (Master) Addr = Block Address (Block), Device Address (Master)
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent lock-bit set operations.

Full status check can be done after each lock-bit set operation or after a sequence of lock-bit set operations.

Write FFH after the last lock-bit set operation to place device in read array mode.

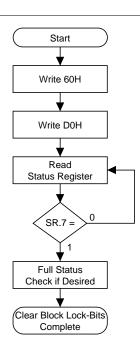
FULL STATUS CHECK PROCEDURE



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR.3 1 = VPP Error Detect
Standby		Check SR.1 1 = Device Protect Detect RP# = VIH (Set Master Lock-Bit Operation) RP# = VIH, Master Lock-Bit is Set (Set Block Lock-Bit Operation)
Standby		Check SR.4, 5 Both 1 = Command Sequence Error
Standby		Check SR.4 1 = Set Lock-Bit Error
SR.5. SR.	4. SR.3 and SI	R.1 are only cleared by the Clear

SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple lock-bits are set before full status is checked.

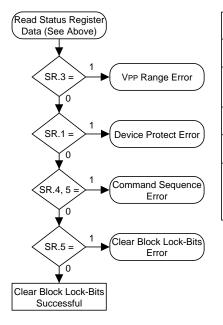
Fig. 7 Set Block and Master Lock-Bit Flowchart



BUS OPERATION	COMMAND	COMMENTS
Write	Clear Block Lock-Bits Setup	Data = 60H Addr = X
Write	Clear Block Lock-Bits Confirm	Data = D0H Addr = X
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Write FFH after the last clear block lock-bits operation to place device in read array mode.

FULL STATUS CHECK PROCEDURE



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR.3 1 = VPP Error Detect
Standby		Check SR.1 1 = Device Protect Detect RP# = VIH, Master Lock-Bit is Set
Standby		Check SR.4, 5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Clear Block Lock-Bits Error

 $\mbox{SR.5}, \mbox{SR.4}, \mbox{SR.3}$ and $\mbox{SR.1}$ are only cleared by the Clear Status Register command.

Fig. 8 Clear Block Lock-Bits Flowchart

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5 DESIGN CONSIDERATIONS

5.1 Three-Line Output Control

The device will often be used in large memory arrays. SHARP provides three control inputs to accommodate multiple memory connections. Three-line control provides for :

- a. Lowest possible memory power consumption.
- b. Complete assurance that data bus contention will not occur.

To use these control inputs efficiently, an address decoder should enable CE# while OE# should be connected to all memory devices and the system's READ# control line. This assures that only selected memory devices have active outputs while deselected memory devices are in standby mode. RP# should be connected to the system POWERGOOD signal to prevent unintended writes during system power transitions. POWERGOOD should also toggle during system reset.

5.2 RY/BY# and Block Erase, Byte Write, and Lock-Bit Configuration Polling

RY/BY# is a full CMOS output that provides a hardware method of detecting block erase, byte write and lock-bit configuration completion. It transitions low after block erase, byte write, or lock-bit configuration commands and returns to VOH when the WSM has finished executing the internal algorithm.

RY/BY# can be connected to an interrupt input of the system CPU or controller. It is active at all times. RY/BY# is also VOH when the device is in block erase suspend (with byte write inactive), byte write suspend or deep power-down modes.

5.3 Power Supply Decoupling

Flash memory power switching characteristics require careful device decoupling. System designers are interested in three supply current issues; standby current levels, active current levels and transient peaks produced by falling and rising edges of CE# and OE#. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 µF ceramic capacitor connected between its Vcc and GND and between its VPP and GND. These high-frequency, low inductance capacitors should be placed as close as possible to package leads. Additionally, for every eight devices, a 4.7 µF electrolytic capacitor should be placed at the array's power supply connection between Vcc and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductance.

5.4 VPP Trace on Printed Circuit Boards

Updating flash memories that reside in the target system requires that the printed circuit board designers pay attention to the VPP power supply trace. The VPP pin supplies the memory cell current for byte writing and block erasing. Use similar trace widths and layout considerations given to the Vcc power bus. Adequate VPP supply traces and decoupling will decrease VPP voltage spikes and overshoots.

5.5 Vcc, VPP, RP# Transitions

Block erase, byte write and lock-bit configuration are not guaranteed if VPP falls outside of a valid VPPH1/2/3 range, VCC falls outside of a valid VCC2/3/4 range, or RP# ≠ VIH or VHH. If VPP error is detected, status register bit SR.3 is set to "1" along with SR.4 or SR.5, depending on the attempted operation. If RP# transitions to VIL during block erase, byte write, or lock-bit configuration, RY/BY# will remain low until the reset operation is complete. Then, the operation will abort and the device will enter deep power-down. The aborted operation may leave data partially altered. Therefore, the command sequence must be repeated after normal

operation is restored. Device power-off or RP# transitions to VIL clear the status register.

The CUI latches commands issued by system software and is not altered by VPP or CE# transitions or WSM actions. Its state is read array mode upon power-up, after exit from deep power-down or after Vcc transitions below VLKO.

After block erase, byte write, or lock-bit configuration, even after VPP transitions down to VPPLK, the CUI must be placed in read array mode via the Read Array command if subsequent access to the memory array is desired.

5.6 Power-Up/Down Protection

The device is designed to offer protection against accidental block erasure, byte writing, or lock-bit configuration during power transitions. Upon power-up, the device is indifferent as to which power supply (VPP or Vcc) powers-up first. Internal circuitry resets the CUI to read array mode at power-up.

A system designer must guard against spurious writes for VCC voltages above VLKO when VPP is active. Since both WE# and CE# must be low for a command write, driving either to VIH will inhibit writes. The CUI's two-step command sequence architecture provides added level of protection against data alteration.

In-system block lock and unlock capability prevents inadvertent data alteration. The device is disabled while RP# = VIL regardless of its control inputs state.

5.7 Power Consumption

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash memory's nonvolatility increases usable battery life because data is retained when system power is removed.

In addition, deep power-down mode ensures extremely low power consumption even when system power is applied. For example, portable computing products and other power sensitive applications that use an array of devices for solid-state storage can consume negligible power by lowering RP# to VIL standby or sleep modes. If access is again needed, the devices can be read following the tPHQV and tPHWL wake-up cycles required after RP# is first raised to VIH. See Section 6.2.4 through 6.2.6 "AC CHARACTERISTICS – READ-ONLY and WRITE OPERATIONS" and Fig. 13, Fig. 14 and Fig. 15 for more information.

6 ELECTRICAL SPECIFICATIONS

6.1 Absolute Maximum Ratings*

Operating Temperature

LH28F002SC-L

During Read, Block Erase, Byte Write and Lock-Bit Configuration 0 to +70°C (NOTE 1)
Temperature under Bias –10 to +80°C

LH28F002SCH-L

Voltage On Any Pin

(except Vcc, Vpp, and RP#)····· −2.0 to +7.0 V (NOTE 3)

Vcc Supply Voltage ····· –2.0 to +7.0 V (NOTE 3)

VPP Update Voltage during

Block Erase, Byte Write and Lock-Bit Configuration ····· -2.0 to +14.0 V (NOTE 3, 4)

RP# Voltage with Respect to

GND during Lock-Bit Configuration

Operations --- -2.0 to +14.0 V (NOTE 3, 4)

Output Short Circuit Current 100 mA (NOTE 5)

NOTICE: The specifications are subject to change without notice. Verify with your local SHARP sales office that you have the latest datasheet before finalizing a design.

*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

NOTE:

- Operating temperature is for commercial product defined by this specification.
- Operating temperature is for extended temperature product defined by this specification.
- All specified voltages are with respect to GND. Minimum DC voltage is -0.5 V on input/output pins and -0.2 V on Vcc and VPP pins. During transitions, this level may undershoot to -2.0 V for periods < 20 ns. Maximum DC voltage on input/output pins and Vcc is Vcc+0.5 V which, during transitions, may overshoot to Vcc+2.0 V for periods < 20 ns.
- Maximum DC voltage on VPP and RP# may overshoot to +14.0 V for periods < 20 ns.
- Output shorted for no more than one second. No more than one output shorted at a time.

6.2 Operating Conditions

SYMBOL	PARAMETER	NOTE	MIN.	MAX.	UNIT	VERSIONS
т.	On agating Tampagatura	4	0	+70	°C	LH28F002SC-L
TA	Operating Temperature	'	-40	+85	°C	LH28F002SCH-L
VCC1	Vcc Supply Voltage (2.7 to 3.6 V)	2	2.7	3.6	V	
VCC2	Vcc Supply Voltage (3.3±0.3 V)		3.0	3.6	V	
Vcc3	Vcc Supply Voltage (5.0±0.25 V)		4.75	5.25	V	LH28F002SC-L85/SCH-L85
VCC4	Vcc Supply Voltage (5.0±0.5 V)		4.50	5.50	V	

- 1. Test condition : Ambient temperature
- 2. Block erase, byte write and lock-bit configuration operations with Vcc < 3.0 V should not be attempted.

6.2.1 CAPACITANCE (NOTE 1)

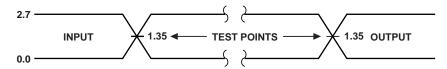
$T_A = +25^{\circ}C$, $f = 1 MHz$

SYMBOL	PARAMETER	TYP.	MAX.	UNIT	CONDITION
CIN	Input Capacitance	6	8	pF	VIN = 0.0 V
Соит	Output Capacitance	8	12	pF	Vout = 0.0 V

NOTE:

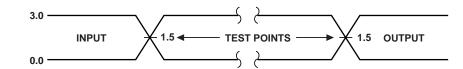
1. Sampled, not 100% tested.

6.2.2 AC INPUT/OUTPUT TEST CONDITIONS



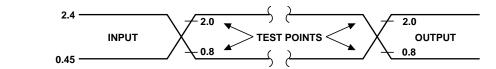
AC test inputs are driven at 2.7 V for a Logic "1" and 0.0 V for a Logic "0". Input timing begins, and output timing ends, at 1.35 V. Input rise and fall times (10% to 90%) < 10 ns.

Fig. 9 Transient Input/Output Reference Waveform for Vcc = 2.7 to 3.6 V



AC test inputs are driven at 3.0 V for a Logic "1" and 0.0 V for a Logic "0". Input timing begins, and output timing ends, at 1.5 V. Input rise and fall times (10% to 90%) < 10 ns.

Fig. 10 Transient Input/Output Reference Waveform for $Vcc = 3.3\pm0.3 \text{ V}$ and $Vcc = 5.0\pm0.25 \text{ V}$ (High Speed Testing Configuration)



AC test inputs are driven at VoH (2.4 VTTL) for a Logic "1" and VoL (0.45 VTTL) for a Logic "0". Input timing begins at VIH (2.0 VTTL) and VIL (0.8 VTTL). Output timing ends at VIH and VIL. Input rise and fall times (10% to 90%) < 10 ns.

Fig. 11 Transient Input/Output Reference Waveform for Vcc = 5.0±0.5 V (Standard Testing Configuration)

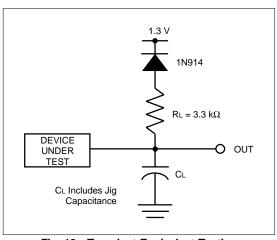


Fig. 12 Transient Equivalent Testing

Load Circuit

Test Configuration Capacitance Loading Value

TEST CONFIGURATION	C∟ (pF)
Vcc = 3.3±0.3 V, 2.7 to 3.6 V	50
Vcc = 5.0±0.25 V (NOTE 1)	30
Vcc = 5.0±0.5 V	100

NOTE:

 Applied to high-speed products, LH28F002SC-L85 and LH28F002SCH-L85.

6.2.3 DC CHARACTERISTICS

CVMDOL	DADAMETED	NOTE	Vcc = 2.7 to 3.6 V Vcc = 3.3		.3±0.3 V	V Vcc = 5.0±0.5 V			TEST	
SYMBOL	PARAMETER	NOTE	TYP.	MAX.	TYP.	MAX.	TYP.	MAX.	UNIT	CONDITIONS
ILI	Input Load Current	1		±0.5		±0.5		±1	μΑ	Vcc = Vcc Max.
									μ., .	VIN = Vcc or GND
ILO	Output Leakage Current	1		±0.5		±0.5		±10	μA	Vcc = Vcc Max.
	, ,								'	Vout = Vcc or GND
			00	400	00	400	0.5	400		CMOS Inputs
			20	100	20	100	25	100	μA	Vcc = Vcc Max.
Iccs	Vcc Standby Current	1, 3, 6								CE# = RP# = Vcc±0.2 V
			0.1	2	0.2	2	0.4	2	mA	TTL Inputs Vcc = Vcc Max.
			0.1		0.2		0.4		IIIA	CE# = RP# = VIH
	LH28F002									OL# - IXF# - VIII
	Vcc Deep Power- SC-L			10		10		10		RP# = GND±0.2 V
ICCD	Down Current LH28F002	1							μΑ	IOUT $(RY/BY#) = 0 mA$
	SCH-L			20		20		20		(,,
										CMOS Inputs
										Vcc = Vcc Max.
			6	12	7	12	17	25	Λ	CE# = GND
			0	12	7	12	17	35	mA	f = 5 MHz (3.3 V, 2.7 V),
										8 MHz (5 V)
ICCR	Vcc Read Current	1, 5, 6								IOUT = 0 mA
ICCR	VCC Read Current	1, 5, 6								TTL Inputs
							20	50	mA	Vcc = Vcc Max.
			7	18	8	18				CE# = GND
			'	10	0	10				f = 5 MHz (3.3 V, 2.7 V),
										8 MHz (5 V)
										Iout = 0 mA
	Vcc Byte Write or			_		17		_	mΑ	VPP = 3.3±0.3 V
Iccw	Set Lock-Bit Current	1, 7		_		17		35	mA	$VPP = 5.0 \pm 0.5 V$
			_	_		12		30	mA	$VPP = 12.0 \pm 0.6 V$
	Vcc Block Erase or					17			mA	$VPP = 3.3 \pm 0.3 \text{ V}$
ICCE	Clear Block Lock-Bits	1, 7		_		17		30	mA	VPP = 5.0±0.5 V
	Current		_			12		25	mA	VPP = 12.0±0.6 V
Iccws	Vcc Byte Write or Block	1, 2	_	_	1	6	1	10	mA	CE# = VIH
ICCES	Erase Suspend Current			45		45		45		\\
IPPS	VPP Standby or	1	±2	±15	±2	±15	±2	±15	μΑ	VPP ≤ VCC
IPPR	Read Current		10	200	10	200	10	200	μΑ	VPP > VCC
IPPD	VPP Deep Power-Down Current	1	0.1	5	0.1	5	0.1	5	μΑ	$RP# = GND \pm 0.2 V$
			_	_		40	_	_	mA	VPP = 3.3±0.3 V
IPPW	VPP Byte Write or Set Lock-Bit Current	1, 7	_	_		40		40	mA	VPP = 5.0±0.5 V
	Set Lock-dit Current		_	_		15		15	mA	VPP = 12.0±0.6 V
	VPP Block Erase or		_	_		20	_	_	mA	VPP = 3.3±0.3 V
IPPE	Clear Block Lock-Bits	1, 7	_	_		20		20	mA	VPP = 5.0±0.5 V
	Current		_	_		15		15	mA	VPP = 12.0±0.6 V
IPPWS	VPP Byte Write or Block	1	_		10	200	10	200	μA	VPP = VPPH1/2/3
IPPES	Erase Suspend Current				.0	200			μ, ,	VII — VIIIII/2/3

6.2.3 DC CHARACTERISTICS (contd.)

SYMBOL	PARAMETER	NOTE	Vcc = 2.7	7 to 3.6 V	Vcc = 3	.3±0.3 V	Vcc = 5	.0±0.5 V	UNIT	TEST
STIVIDUL	PARAMETER	NOIE	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNII	CONDITIONS
VIL	Input Low Voltage	7	-0.5	0.8	-0.5	0.8	-0.5	0.8	V	
VIH	Input High Voltage	7	2.0	Vcc +0.5	2.0	Vcc +0.5	2.0	Vcc +0.5	V	
Vol	Output Low Voltage	3, 7		0.4		0.4		0.45	V	Vcc = Vcc Min. IoL = 5.8 mA (5 V) IoL = 2.0 mA (3.3 V, 2.7 V)
Vон1	Output High Voltage (TTL)	3, 7	2.4		2.4		2.4		V	$V_{CC} = V_{CC}$ Min. $I_{OH} = -2.5$ mA (5 V) $I_{OH} = -2.0$ mA (3.3 V, 2.7 V)
	Output High Voltage		0.85 Vcc		0.85 Vcc		0.85 Vcc		V	$V_{CC} = V_{CC} Min.$ $I_{OH} = -2.5 mA$
VOH2	(CMOS)	3, 7	Vcc -0.4		Vcc -0.4		Vcc -0.4		V	Vcc = Vcc Min. IoH = -100 μA
VPPLK	VPP Lockout Voltage during Normal Operations	4, 7		1.5		1.5		1.5	V	
VPPH1	VPP Voltage during Byte Write, Block Erase or Lock-Bit Operations			_	3.0	3.6	_	_	V	
VPPH2	VPP Voltage during Byte Write, Block Erase or Lock-Bit Operations		_	_	4.5	5.5	4.5	5.5	V	
VPPH3	or Lock-Bit Operations		_	_	11.4	12.6	11.4	12.6	V	
VLKO	Vcc Lockout Voltage		2.0		2.0		2.0		V	
Vнн	RP# Unlock Voltage	8, 9	_	_	11.4	12.6	11.4	12.6	V	Set master lock-bit Override master and block lock-bit

- All currents are in RMS unless otherwise noted. Typical values at nominal Vcc voltage and TA = +25°C. These currents are valid for all product versions (packages and speeds).
- Iccws and Icces are specified with the device deselected. If reading or byte writing in erase suspend mode, the device's current draw is the sum of Iccws or Icces and IccR or Iccw, respectively.
- 3. Includes RY/BY#.
- Block erases, byte writes, and lock-bit configurations are inhibited when VPP ≤ VPPLK, and not guaranteed in the range between VPPLK (max.) and VPPH1 (min.), between VPPH1 (max.) and VPPH2 (min.), between VPPH2 (max.) and VPPH3 (min.), and above VPPH3 (max.).
- Automatic Power Saving (APS) reduces typical IccR to 1 mA at 5 V Vcc and 3 mA at 2.7 V and 3.3 V Vcc in static operation.

- CMOS inputs are either Vcc±0.2 V or GND±0.2 V. TTL inputs are either Vi∟ or Viн.
- 7. Sampled, not 100% tested.
- 8. Master lock-bit set operations are inhibited when RP# = VIH. Block lock-bit configuration operations are inhibited when the master lock-bit is set and RP# = VIH. Block erases and byte writes are inhibited when the corresponding block lock-bit is set and RP# = VIH. Block erase, byte write, and lock-bit configuration operations are not guaranteed with Vcc < 3.0 V or VIH < RP# < VHH and should not be attempted.</p>
- RP# connection to a VHH supply is allowed for a maximum cumulative period of 80 hours.

6.2.4 AC CHARACTERISTICS - READ-ONLY OPERATIONS (NOTE 1)

• Vcc = 2.7 to 3.6 V, TA = 0 to 70°C or -40 to +85°C

	VERSIONS		2SC-L85 2SCH-L85	LH28F00 LH28F002	UNIT		
SYMBOL	PARAMETER	NOTE	MIN.	MAX.	MIN.	MAX.	
tavav	Read Cycle Time		150		170		ns
tavqv	Address to Output Delay			150		170	ns
telqv	CE# to Output Delay	2		150		170	ns
tphqv	RP# High to Output Delay			600		600	ns
tGLQV	OE# to Output Delay	2		50		55	ns
tELQX	CE# to Output in Low Z	3	0		0		ns
tehqz	CE# High to Output in High Z	3		55		55	ns
tGLQX	OE# to Output in Low Z	3	0		0		ns
tghqz	OE# High to Output in High Z	3		20		25	ns
tон	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		0		ns

• Vcc = 3.3±0.3 V, TA = 0 to +70°C or -40 to +85°C

	VERSIONS)2SC-L85 2SCH-L85)2SC-L12 2SCH-L12	UNIT
SYMBOL	PARAMETER	NOTE	MIN.	MAX.	MIN.	MAX.	1
tavav	Read Cycle Time		120		150		ns
tavqv	Address to Output Delay			120		150	ns
tELQV	CE# to Output Delay	2		120		150	ns
tphqv	RP# High to Output Delay			600		600	ns
tGLQV	OE# to Output Delay	2		50		55	ns
tELQX	CE# to Output in Low Z	3	0		0		ns
tehqz	CE# High to Output in High Z	3		55		55	ns
tGLQX	OE# to Output in Low Z	3	0		0		ns
tghqz	OE# High to Output in High Z	3		20		25	ns
tон	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		0		ns

- 1. See AC Input/Output Reference Waveform (Fig. 9 through Fig. 11) for maximum allowable input slew rate.
- 2. OE# may be delayed up to tELQV-tGLQV after the falling edge of CE# without impact on tELQV.
- 3. Sampled, not 100% tested.

6.2.4 AC CHARACTERISTICS - READ-ONLY OPERATIONS (contd.) (NOTE 1)

• Vcc = 5.0±0.25 V, 5.0±0.5 V, TA = 0 to +70°C or -40 to +85°C

	VERSIONS		±0.25 V)2SC-L85 2SCH-L85					
	VERSIONS	Vcc:	±0.5 V)2SC-L85 2SCH-L85	(NOTE 5) 5 LH28F002SC-L1 35 LH28F002SCH-L		UNIT
SYMBOL	PARAMETER		NOTE	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tavav	Read Cycle Time			85		90		120		ns
tavqv	Address to Output Delay				85		90		120	ns
tELQV	CE# to Output Delay		2		85		90		120	ns
t PHQV	RP# High to Output Delay				400		400		400	ns
tGLQV	OE# to Output Delay		2		40		45		50	ns
tELQX	CE# to Output in Low Z		3	0		0		0		ns
tehqz	CE# High to Output in High 2	Z	3		55		55		55	ns
tGLQX	OE# to Output in Low Z		3	0		0		0		ns
tghqz	OE# High to Output in High 2	z	3		10		10		15	ns
	Output Hold from Address,									
tон	CE# or OE# Change,		3	0		0		0		ns
	Whichever Occurs First									

- See AC Input/Output Reference Waveform (Fig. 9 through Fig. 11) for maximum allowable input slew rate.
- OE# may be delayed up to tELQV-tGLQV after the falling edge of CE# without impact on tELQV.
- 3. Sampled, not 100% tested.
- See Fig. 10 "Transient Input/Output Reference Waveform" and Fig. 12 "Transient Equivalent Testing Load Circuit" (High Speed Configuration) for testing characteristics.
- See Fig. 11 "Transient Input/Output Reference Waveform" and Fig. 12 "Transient Equivalent Testing Load Circuit" (Standard Configuration) for testing characteristics.

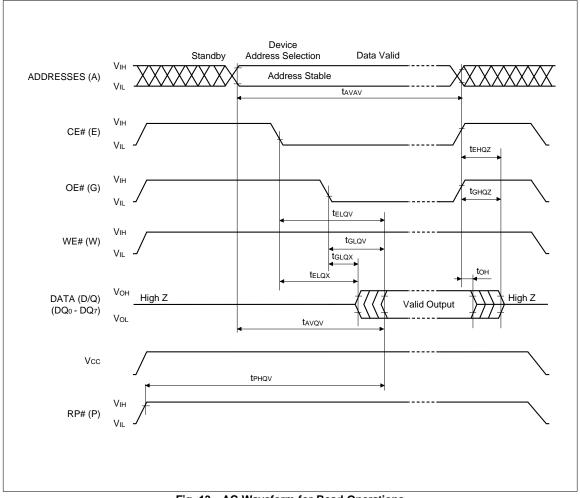


Fig. 13 AC Waveform for Read Operations

6.2.5 AC CHARACTERISTICS - WRITE OPERATION (NOTE 1)

• Vcc = 2.7 to 3.6 V, TA = 0 to +70°C or -40 to +85°C

	VERSIONS		2SC-L85 2SCH-L85)2SC-L12 2SCH-L12	UNIT	
SYMBOL	PARAMETER	NOTE	MIN.	MAX.	MIN.	MAX.	
tavav	Write Cycle Time		150		170		ns
tphwl	RP# High Recovery to WE# Going Low	2	1		1		μs
telwl	CE# Setup to WE# Going Low		10		10		ns
twLwH	WE# Pulse Width		50		50		ns
tavwh	Address Setup to WE# Going High	3	50		50		ns
tovwh	Data Setup to WE# Going High	3	50		50		ns
twhdx	Data Hold from WE# High		5		5		ns
twhax	Address Hold from WE# High		5		5		ns
twheh	CE# Hold from WE# High		10		10		ns
twhwL	WE# Pulse Width High		30		30		ns
twhgl	Write Recovery before Read		0		0		ns

• Vcc = 3.3±0.3 V, TA = 0 to +70°C or -40 to +85°C

	VERSIONS)2SC-L85 2SCH-L85)2SC-L12 2SCH-L12	UNIT
SYMBOL	PARAMETER	NOTE	MIN.	MAX.	MIN.	MAX.	
tavav	Write Cycle Time		120		150		ns
tPHWL	RP# High Recovery to WE# Going Low	2	1		1		μs
tELWL	CE# Setup to WE# Going Low		10		10		ns
twLwH	WE# Pulse Width		50		50		ns
tphhwh	RP# VHH Setup to WE# Going High	2	100		100		ns
tvpwh	VPP Setup to WE# Going High	2	100		100		ns
tavwh	Address Setup to WE# Going High	3	50		50		ns
tovwh	Data Setup to WE# Going High	3	50		50		ns
twhdx	Data Hold from WE# High		5		5		ns
twhax	Address Hold from WE# High		5		5		ns
twheh	CE# Hold from WE# High		10		10		ns
twhwl	WE# Pulse Width High		30		30		ns
twhrl	WE# High to RY/BY# Going Low			100		100	ns
twhgl	Write Recovery before Read		0		0		ns
tQVVL	VPP Hold from Valid SRD, RY/BY# High	2, 4	0		0		ns
tQVPH	RP# VHH Hold from Valid SRD, RY/BY# High	2, 4	0		0		ns

- Read timing characteristics during block erase, byte write and lock-bit configuration operations are the same as during read-only operations. Refer to Section 6.2.4 "AC CHARACTERISTICS" for read-only operations.
- 2. Sampled, not 100% tested.

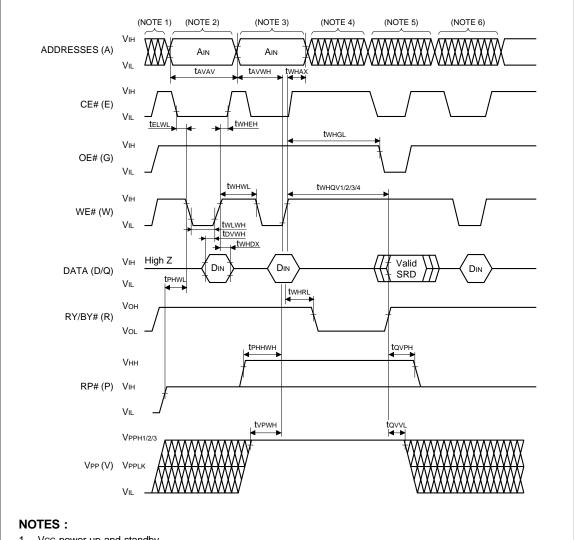
- 3. Refer to **Table 3** for valid AIN and DIN for block erase, byte write, or lock-bit configuration.
- VPP should be held at VPPH1/2/3 (and if necessary RP# should be held at VHH) until determination of block erase, byte write, or lock-bit configuration success (SR.1/3/4/5 = 0).

6.2.5 AC CHARACTERISTICS - WRITE OPERATION (contd.) (NOTE 1)

• Vcc = 5.0±0.25 V, 5.0±0.5 V, TA = 0 to +70°C or -40 to +85°C

	VERSIONS	Vcc±(0.25 V	(NOTE 5) LH28F00 LH28F002	2SC-L85 2SCH-L85					
		Vcc±	.0.5 V			(NOTE 6) LH28F002SC-L85 LH28F002SCH-L85		(NOTE 6) LH28F002SC-L12 LH28F002SCH-L12		UNIT
SYMBOL	PARAMETER	1	NOTE	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tavav	Write Cycle Time			85		90		120		ns
tPHWL	RP# High Recovery to WE# Going Low		2	1		1		1		μs
telwl	CE# Setup to WE# Going Lo	w		10		10		10		ns
twLwH	WE# Pulse Width			40		40		40		ns
tphhwh	RP# VHH Setup to WE# Going H	ligh	2	100		100		100		ns
t∨pwh	VPP Setup to WE# Going Hig	ıh	2	100		100		100		ns
tavwh	Address Setup to WE# Going Hi	igh	3	40		40		40		ns
to∨wн	Data Setup to WE# Going High	gh	3	40		40		40		ns
twhdx	Data Hold from WE# High			5		5		5		ns
twhax	Address Hold from WE# High	1		5		5		5		ns
twheh	CE# Hold from WE# High			10		10		10		ns
twhwl	WE# Pulse Width High			30		30		30		ns
twhrl	WE# High to RY/BY# Going Lo	ow			90		90		90	ns
twhgl	Write Recovery before Read			0		0		0		ns
tQVVL	VPP Hold from Valid SRD, RY/BY# High		2, 4	0		0		0		ns
tQVPH	RP# V _{HH} Hold from Valid SR RY/BY# High	D,	2, 4	0		0		0		ns

- Read timing characteristics during block erase, byte write and lock-bit configuration operations are the same as during read-only operations. Refer to Section 6.2.4 "AC CHARACTERISTICS" for read-only operations.
- 2. Sampled, not 100% tested.
- Refer to Table 3 for valid AIN and DIN for block erase, byte write, or lock-bit configuration.
- VPP should be held at VPPH1/2/3 (and if necessary RP# should be held at VHH) until determination of block erase, byte write, or lock-bit configuration success (SR.1/3/4/5 = 0).
- See Fig. 10 "Transient Input/Output Reference Waveform" and Fig. 12 "Transient Equivalent Testing Load Circuit" (High Seed Configuration) for testing characteristics.
- See Fig. 11 "Transient Input/Output Reference Waveform" and Fig. 12 "Transient Equivalent Testing Load Circuit" (Standard Configuration) for testing characteristics.



- 1. Vcc power-up and standby.
- 2. Write block erase or byte write setup.
- 3. Write block erase confirm or valid address and data.
- 4. Automated erase or program delay.
- Read status register data.
- Write Read Array command.

Fig. 14 AC Waveform for WE#-Controlled Write Operations

6.2.6 ALTERNATIVE CE#-CONTROLLED WRITES (NOTE 1)

• Vcc = 2.7 to 3.6 V, TA = 0 to +70°C or -40 to +85°C

	VERSIONS)2SC-L85 2SCH-L85		2SC-L12 2SCH-L12	UNIT	
SYMBOL	PARAMETER	NOTE	MIN.	MAX.	MIN.	MAX.	
tavav	Write Cycle Time		150		170		ns
tphel	RP# High Recovery to CE# Going Low	2	1		1		μs
twlel	WE# Setup to CE# Going Low		0		0		ns
teleh	CE# Pulse Width		70		70		ns
taveh	Address Setup to CE# Going High	3	50		50		ns
toveh	Data Setup to CE# Going High	3	50		50		ns
tehdx	Data Hold from CE# High		5		5		ns
tehax	Address Hold from CE# High		5		5		ns
tehwh	WE# Hold from CE# High		0		0		ns
tehel	CE# Pulse Width High		25		25		ns
tEHGL	Write Recovery before Read		0		0		ns

• Vcc = 3.3±0.3 V, TA = 0 to +70°C or -40 to +85°C

	VERSIONS)2SC-L85	LH28F00		
				2SCH-L85		2SCH-L12	UNIT
SYMBOL	PARAMETER	NOTE	MIN.	MAX.	MIN.	MAX.	
tavav	Write Cycle Time		120		150		ns
tPHEL	RP# High Recovery to CE# Going Low	2	1		1		μs
twlel	WE# Setup to CE# Going Low		0		0		ns
teleh	CE# Pulse Width		70		70		ns
tphheh	RP# V _{HH} Setup to CE# Going High	2	100		100		ns
t∨PEH	VPP Setup to CE# Going High	2	100		100		ns
taveh	Address Setup to CE# Going High	3	50		50		ns
toveh	Data Setup to CE# Going High	3	50		50		ns
tehdx	Data Hold from CE# High		5		5		ns
tehax	Address Hold from CE# High		5		5		ns
tehwh	WE# Hold from CE# High		0		0		ns
tehel	CE# Pulse Width High		25		25		ns
tehrl	CE# High to RY/BY# Going Low			100		100	ns
tehgl	Write Recovery before Read		0		0		ns
tqvvl	VPP Hold from Valid SRD, RY/BY# High	2, 4	0		0		ns
tQVPH	RP# VHH Hold from Valid SRD, RY/BY# High	2, 4	0		0		ns

- In systems where CE# defines the write pulse width (within a longer WE# timing waveform), all setup, hold, and inactive WE# times should be measured relative to the CE# waveform.
- 2. Sampled, not 100% tested.

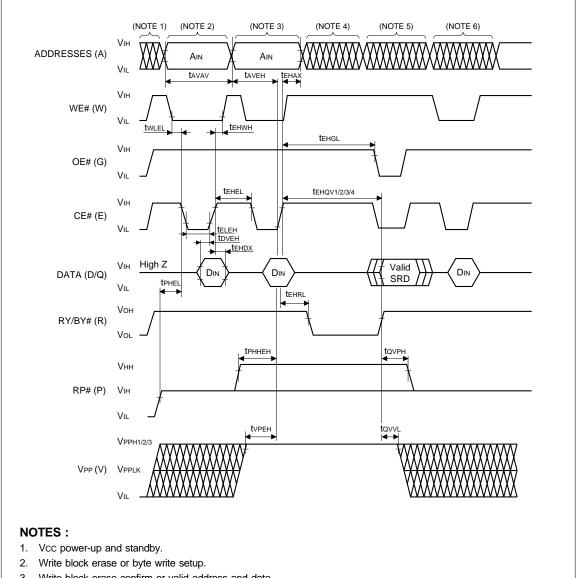
- 3. Refer to **Table 3** for valid AIN and DIN for block erase, byte write, or lock-bit configuration.
- VPP should be held at VPPH1/2/3 (and if necessary RP# should be held at VHH) until determination of block erase, byte write, or lock-bit configuration success (SR.1/3/4/5 = 0).

6.2.6 ALTERNATIVE CE#-CONTROLLED WRITES (contd.) (NOTE 1)

• Vcc = 5.0±0.25 V, 5.0±0.5 V, TA = 0 to +70°C or -40 to +85°C

	VERSIONS	/cc±0.25	i V	1)2SC-L85 2SCH-L85					
		Vcc±0.5 V)2SC-L85 2SCH-L85)2SC-L12 2SCH-L12	UNIT
SYMBOL	PARAMETER	NO.	ΤE	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tavav	Write Cycle Time			85		90		120		ns
tPHEL	RP# High Recovery to CE# Going Low	2		1		1		1		μs
twlel	WE# Setup to CE# Going Lov	v		0		0		0		ns
teleh	CE# Pulse Width			50		50		50		ns
tphheh	RP# VHH Setup to CE# Going High	gh 2		100		100		100		ns
tvpeh	VPP Setup to CE# Going High	2		100		100		100		ns
taveh	Address Setup to CE# Going Hig	h 3	,	40		40		40		ns
tdveh	Data Setup to CE# Going Hig	h 3	,	40		40		40		ns
tehdx	Data Hold from CE# High			5		5		5		ns
tehax	Address Hold from CE# High			5		5		5		ns
tehwh	WE# Hold from CE# High			0		0		0		ns
tehel	CE# Pulse Width High			25		25		25		ns
tehrl	CE# High to RY/BY# Going Lo	ow			90		90		90	ns
tehgl	Write Recovery before Read			0		0		0		ns
tQVVL	VPP Hold from Valid SRD, RY/BY# High	2,	4	0		0		0		ns
tQVPH	RP# VHH Hold from Valid SRI RY/BY# High	2,	4	0		0		0		ns

- In systems where CE# defines the write pulse width (within a longer WE# timing waveform), all setup, hold, and inactive WE# times should be measured relative to the CE# waveform.
- 2. Sampled, not 100% tested.
- Refer to Table 3 for valid AIN and DIN for block erase, byte write, or lock-bit configuration.
- VPP should be held at VPPH1/2/3 (and if necessary RP# should be held at VHH) until determination of block erase, byte write, or lock-bit configuration success (SR.1/3/4/5 = 0).
- See Fig. 10 "Transient Input/Output Reference Waveform" and Fig. 12 "Transient Equivalent Testing Load Circuit" (High Seed Configuration) for testing characteristics.
- See Fig. 11 "Transient Input/Output Reference Waveform" and Fig. 12 "Transient Equivalent Testing Load Circuit" (Standard Configuration) for testing characteristics.



- 3. Write block erase confirm or valid address and data.
- 4. Automated erase or program delay.
- 5. Read status register data.
- 6. Write Read Array command.

Fig. 15 AC Waveform for CE#-Controlled Write Operations

6.2.7 RESET OPERATIONS

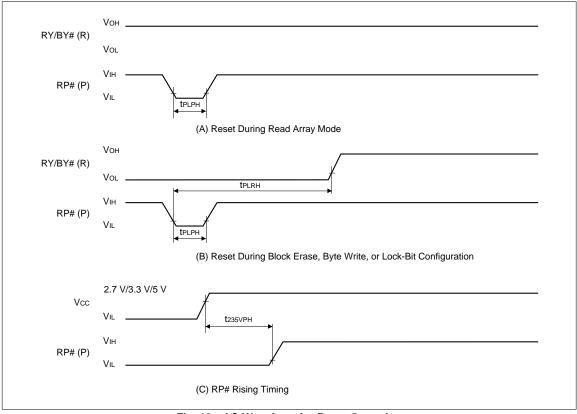


Fig. 16 AC Waveform for Reset Operation

Reset AC Specifications (NOTE 1)

CVMDOL	PARAMETER	NOTE	Vcc = 2.7 to 3.6 V		$Vcc = 3.3 \pm 0.3 \text{ V}$		$Vcc = 5.0\pm0.5 \text{ V}$		UNIT
SYMBOL	PARAMETER	NOIE	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	וואטן
	RP# Pulse Low Time								
tplph	(If RP# is tied to Vcc, this		100		100		100		ns
	specification is not applicable)								
	RP# Low to Reset during								
tplrh	Block Erase, Byte Write or	2, 3		_		20		12	μs
	Lock-Bit Configuration								
	Vcc 2.7 V to RP# High								
t235VPH	Vcc 3.0 V to RP# High	4	100		100		100		ns
	Vcc 4.5 V to RP# High								

- These specifications are valid for all product versions (packages and speeds).
- If RP# is asserted while a block erase, byte write, or lock-bit configuration operation is not executing, the reset will complete within 100 ns.
- A reset time, tPHQV, is required from the latter of RY/BY# or RP# going high until outputs are valid.
- 4. When the device power-up, holding RP#-low minimum 100 ns is required after Vcc has been in predefined range and also has been in stable there.

6.2.8 BLOCK ERASE, BYTE WRITE AND LOCK-BIT CONFIGURATION PERFORMANCE (NOTE 3, 4)

• Vcc = 3.3±0.3 V, TA = 0 to +70°C or -40 to +85°C

CVMDOL	DADAMETED	NOTE	V _{PP}	$= 3.3 \pm 0$.3 V	V _{PP}	= 5.0±0	.5 V	$V_{PP} = 12.0 \pm 0.6 \text{ V}$			
SYMBOL	PARAMETER	NOTE	MIN.	TYP.(NOTE 1)	MAX.	MIN.	TYP.(NOTE 1)	MAX.	MIN.	TYP.(NOTE 1)	MAX.	UNIT
tWHQV1	Byte Write Time	2	15	17	TBD	8.2	9.3	TBD	6.7	7.6	TBD	
tEHQV1	byte write fille		13	17	טסו	0.2	9.3	טסו	0.7	7.0	ושטו	μs
	Block Write Time	2	1	1.1	TBD	0.5	0.5	TBD	0.4	0.5	TBD	S
tWHQV2	Block Erase Time	2	1.5	1.8	TBD	1	1.2	TBD	0.8	1.1	TBD	s
tEHQV2	DIOCK ETASE TITLE		1.5	1.0	טסו	'	1.2	טסו	0.6	1.1	ושטו	5
twhqv3	Set Lock-Bit Time	2	18	21	TBD	11.2	13.3	TBD	9.7	11.6	TBD	
tEHQV3	Set Lock-bit Time		10	21	טסו	11.2	13.3	טסו	9.7	11.0	טסו	μs
tWHQV4	Clear Block Lock-Bits	2	1.5	1.8	TBD	1	1.2	TBD	0.8	1.1	TBD	
tEHQV4	Time		1.5	1.0	טסו	1	1.2	עסו	0.0	1.1	עסו	S
twhrh1	Byte Write Suspend			7.1	10		6.6	9.3		7.4	10.4	
tEHRH1	Latency Time to Read			7.1	10		0.6	9.3		7.4	10.4	μs
tWHRH2	Erase Suspend Latency			15.2	21.1		12.3	17.2		12.3	17.2	
tEHRH2	Time to Read			15.2	Z1.1		12.3	17.2		12.3	17.2	μs

• Vcc = 5.0±0.25 V, 5.0±0.5 V, TA = 0 to +70°C or -40 to +85°C

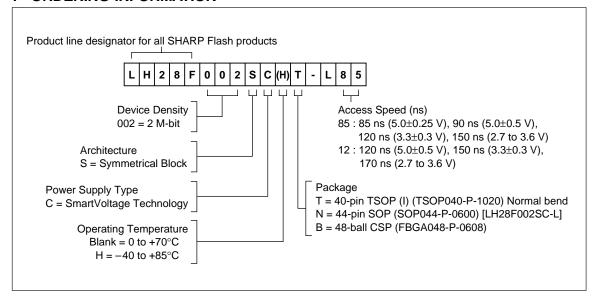
CVMDOL	DADAMETED	NOTE	VPP	$= 5.0\pm0$.5 V	VPP	= 12.0±0	0.6 V	
SYMBOL	PARAMETER	NOTE	MIN.	TYP.(NOTE 1)	MAX.	MIN.	TYP.(NOTE 1)	MAX.	UNIT
twhqv1	Di da Mrida Tiran	2	C.F.	8	TBD	4.0	_	TBD	
tehqv1	Byte Write Time	2	6.5	8	עמו	4.8	6	טפו	μs
	Block Write Time	2	0.4	0.5	TBD	0.3	0.4	TBD	s
twhqv2	Block Erase Time	2	0.0	4.4	TBD	0.0	4.0	TBD	
tEHQV2	BIOCK Erase Time	2	0.9	1.1	עמו	0.3	1.0	טפו	S
twhqv3	Set Lock-Bit Time	2	9.5	12	TBD	7.8	10	TBD	
tehqv3	Set Lock-bit Time		9.5	12	עסו	1.0	10	עסו	μs
twhqv4	Clear Block Lock-Bits Time	2	0.9	1.1	TBD	0.3	1.0	TBD	s
tehqv4	Clear Block Lock-Bits Time		0.9	1.1	טסו	0.5	1.0	טסו	5
twhrh1	Puta Write Suspend Latency Time to Bond			5.6	7		5.2	7.5	
tehrh1	Byte Write Suspend Latency Time to Read			5.6	'		5.2	7.5	μs
twhrh2	France Supposed Latency Time to Board			9.4	13.1		9.8	12.6	
tehrh2	Erase Suspend Latency Time to Read			9.4	13.1		9.8	12.6	μs

- Typical values measured at TA = +25°C and nominal voltages. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
- 2. Excludes system-level overhead.

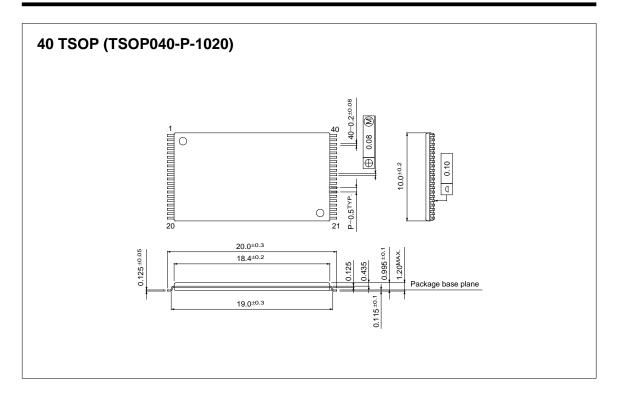
- These performance numbers are valid for all speed versions.
- 4. Sampled, not 100% tested.

LH28F002SC-L/SCH-L

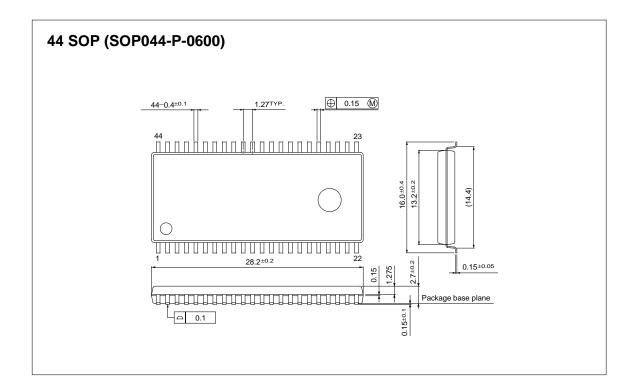
7 ORDERING INFORMATION



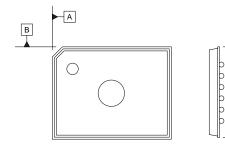
		VALID OPERATIONAL COMBINATIONS							
ODTION	ODDED CODE	Vcc = 2.7 to 3.6 V	cc = 2.7 to 3.6 V Vcc = 3.3±0.3 V Vc		$Vcc = 5.0 \pm 0.25 V$				
OPTION	ORDER CODE	50 pF load,	50 pF load,	100 pF load,	30 pF load,				
		1.35 V I/O Levels	1.5 V I/O Levels	TTL I/O Levels	1.5 V I/O Levels				
1	LH28F002SCXX-L85	150 ns	120 ns	90 ns	85 ns				
2	LH28F002SCXX-L12	170 ns	150 ns	120 ns					

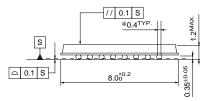


SHARP PACKAGING



48 CSP (FBGA048-P-0608)





*Land hole diameter for ball mounting

 $6.0^{+0.2}_{0}$

